WHAT IS CLAIMED IS:

1. A chip-on-glass type liquid crystal display (LCD), comprising:

an LCD panel having a plurality of pixels;

a plurality of source driving sections connected in series by first panel wiring formed on the LCD panel, supplied with a driving voltage through the first panel wiring, generating contrast voltages corresponding to data to be displayed on the LCD panel, and providing the generated contrast voltages to the LCD panel; and

a plurality of gate driving sections connected in series by second panel wiring formed on the LCD panel, supplied with a driving voltage through the second panel wiring, and scanning the plurality of pixels of the LCD panel sequentially row by row,

wherein each of the plurality of source driving sections increases and outputs an inputted source driving voltage to make a leading source driving voltage equal to a trailing source driving voltage, while each of the plurality of gate driving sections increases and outputs an inputted gate driving voltage to make a leading gate driving voltage equal to a trailing gate driving voltage.

2. A chip-on-glass type LCD as claimed in claim 1, wherein each of the gate driving sections comprises a charge pumping circuit for increasing the leading gate driving voltage to a predetermined level, and a buffer circuit for stabilizing an output voltage of the charge pumping circuit.

3. A chip-on-glass type LCD as claimed in claim 1, wherein each of the source driving sections comprises a charge pumping circuit for increasing the leading source driving voltage to a predetermined level, and a buffer circuit for stabilizing an output voltage of the charge pumping circuit.

4. A chip-on-glass type LCD as claimed in claim 2 or 3, wherein the buffer circuit includes two CMOS (Complementary Metal Oxide Semiconductors) inverters connected with each other in series; and wherein the output voltage of the charge pumping circuit is used as an input voltage and a driving voltage of the buffer circuit.

5. A chip-on-glass type LCD as claimed in claim 2, wherein the first panel wiring has a resistance value adjusted according to an output voltage of the buffer circuit

and process parameters of a length, a width and a thickness of the first panel wiring.

6. A chip-on-glass type LCD as claimed in claim 3, wherein the second panel wiring has a resistance value adjusted according to an output voltage of the buffer circuit and process parameters of a length, a width and a thickness of the second panel wiring.